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MS-7276 uATX Version: 13

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe family processors in LGA775 Package.

System Chipset:

Intel BroadwaterG965/Q965 (North Bridge)
Intel ICH8DO / DH (South Bridge)

On Board Device:

BIOS -- SPI Flash 8M
Azalia Codec -- ALC883
LPC Super I/O -- W83627DHG
LAN -- NINEVEH/EKRON
CLOCK Gen -- ICS 9LPR502 (56pin)
1394 Controller -- VT6307 (2-port)
Hi-USB to PATA Bridge -- JM20335

Main Memory:

Dual-channel DDR-II * 4 (Max 4GB)


Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

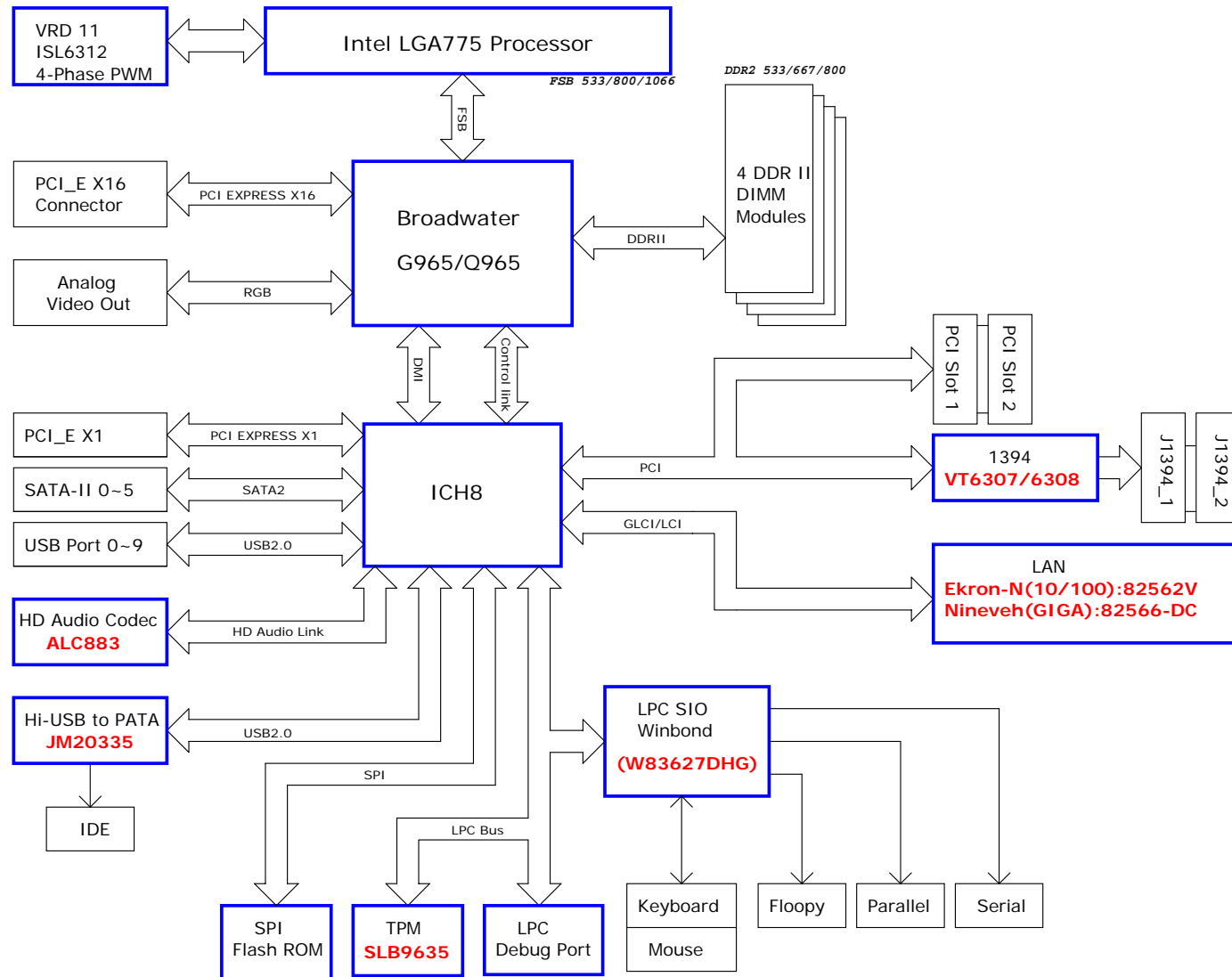
Intersil PWM:

Controller: Intersil ISL6312 (4 Phases)
Driver: Intersil ISL6612

Option	Function	Orcad Configure	BOM
STD	Broadwater/ICH8/W83627DHG/ALC883/82566DM/USB to IDE	cfg-STD	601-7276-A10
OPT:B	Broadwater/ICH8/W83627DHG/ALC883/82562V/USB to IDE	cfg-82562V	601-7276-A20
OPT:C	G965/ICH8DH/W83627DHG/ALC883/82566DC/JM20335	cfg-82566DC	601-7276-01S
OPT:D	Q965/ICH8DO/W83627DHG/ALC883/82566DM/JM20335	cfg-STD	601-7276-03S

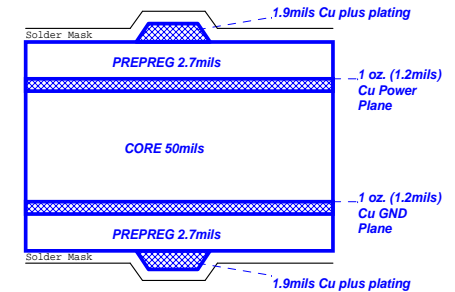
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				MS-7276			
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Block Diagram



Board Stack-up

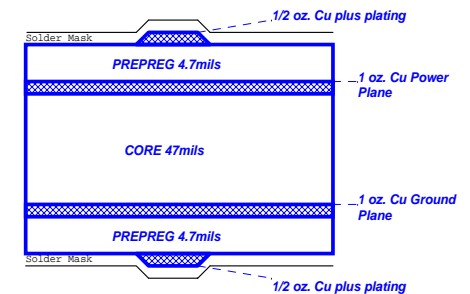
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils
 IEEE1394 - 110ohm Top : 5/7/5
 PCIE, LAN, SATA - 100ohm Top : 5/6/5
 USB2.0 - 90ohm Top : 7.5/7.5/7.5

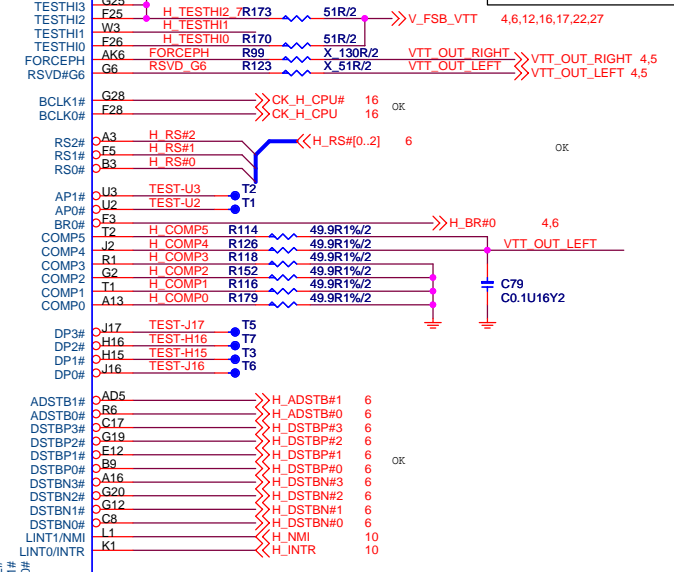
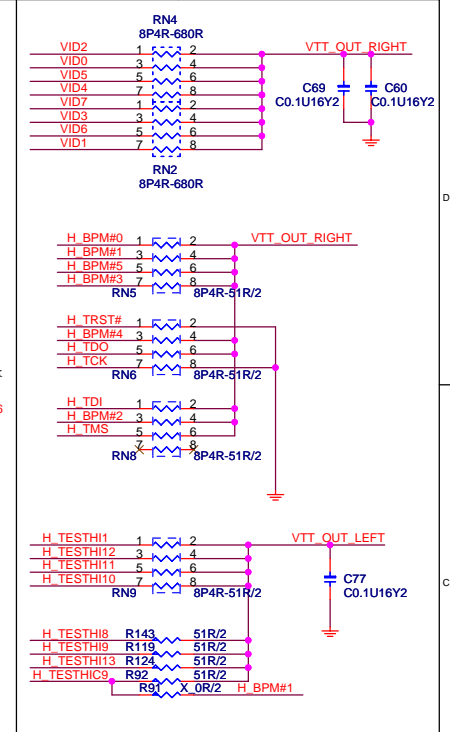
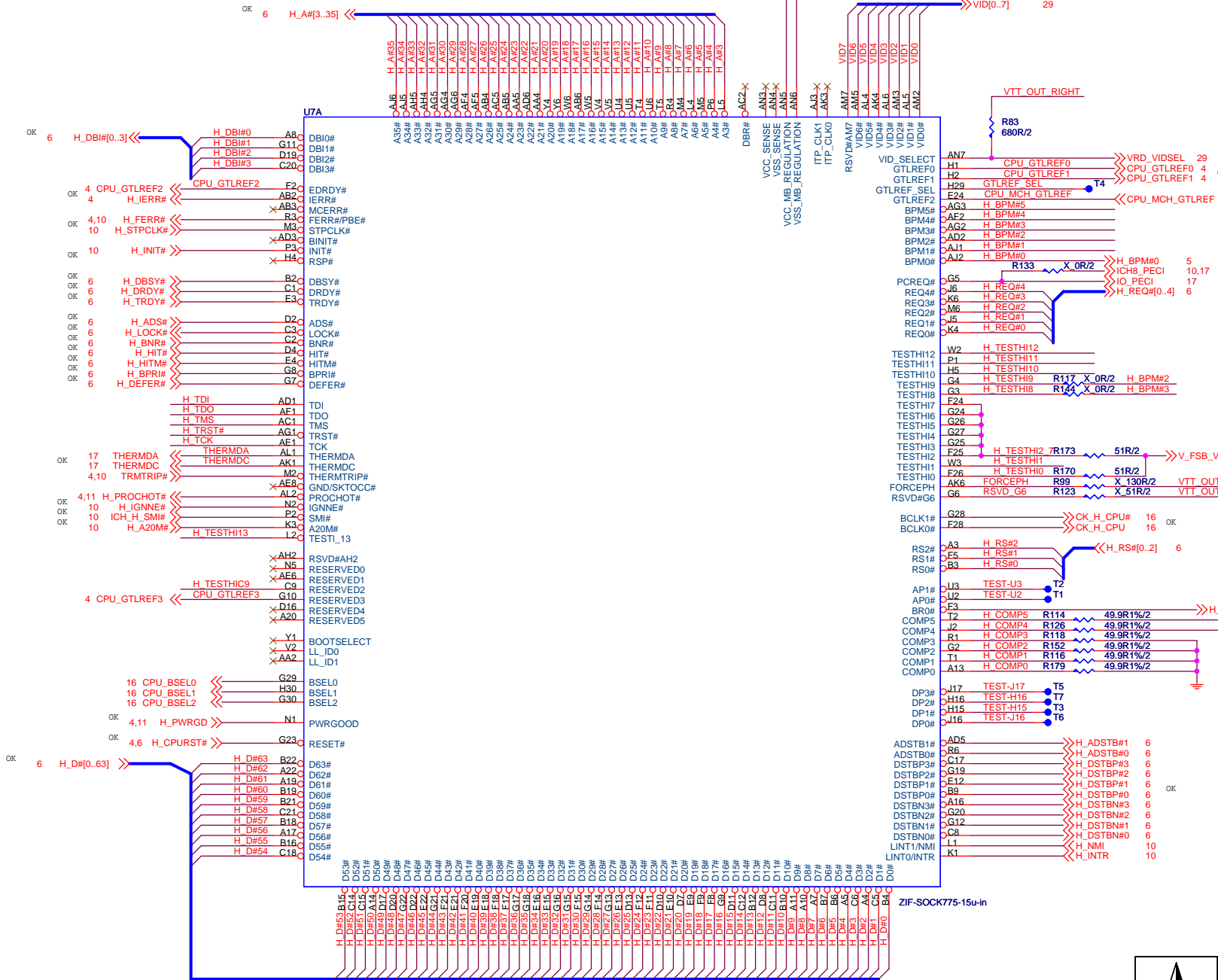


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CPU SIGNAL BLOCK

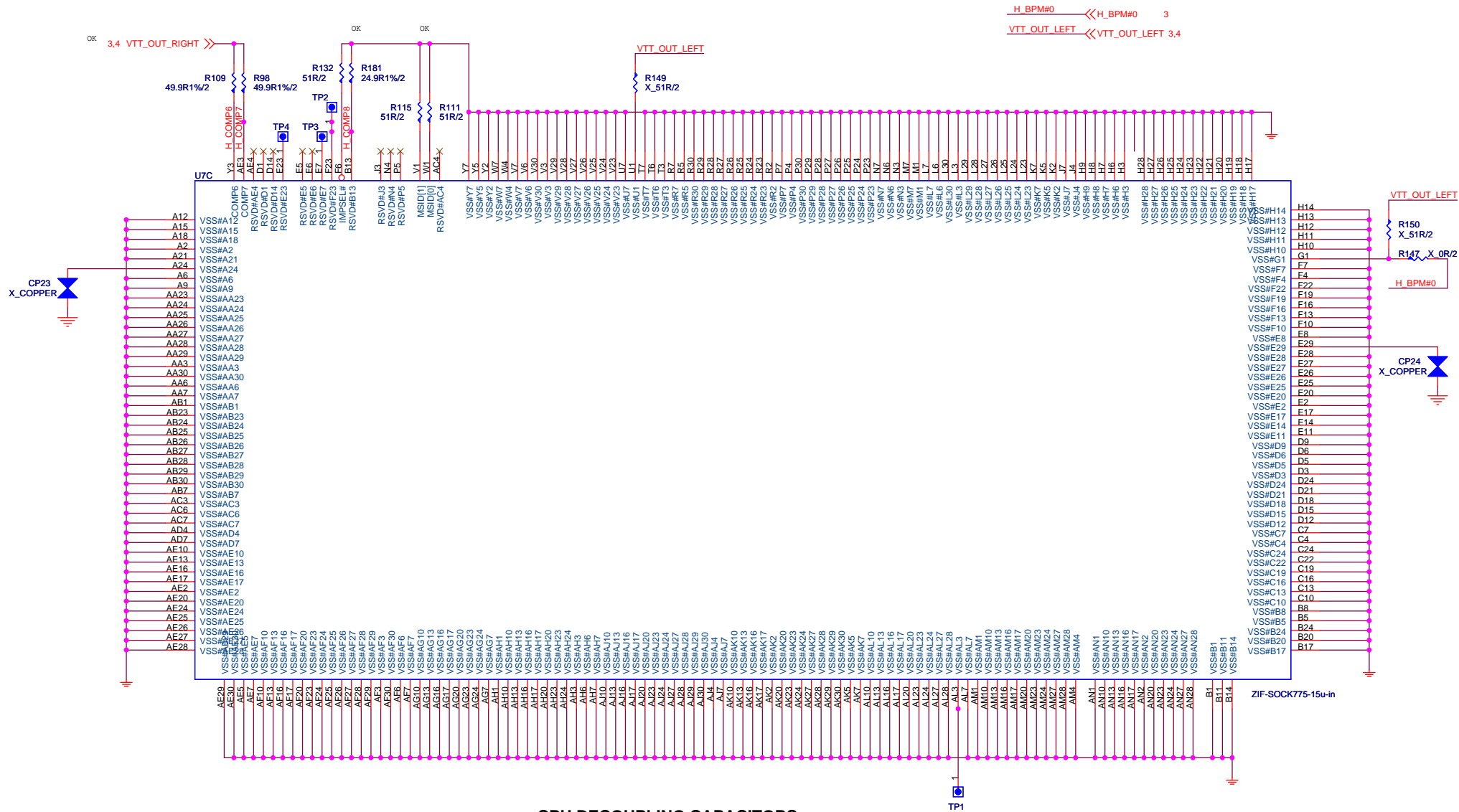


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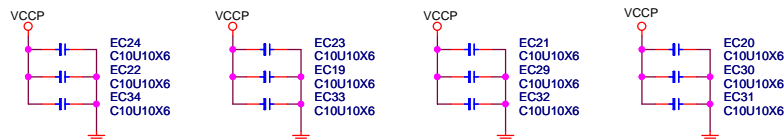
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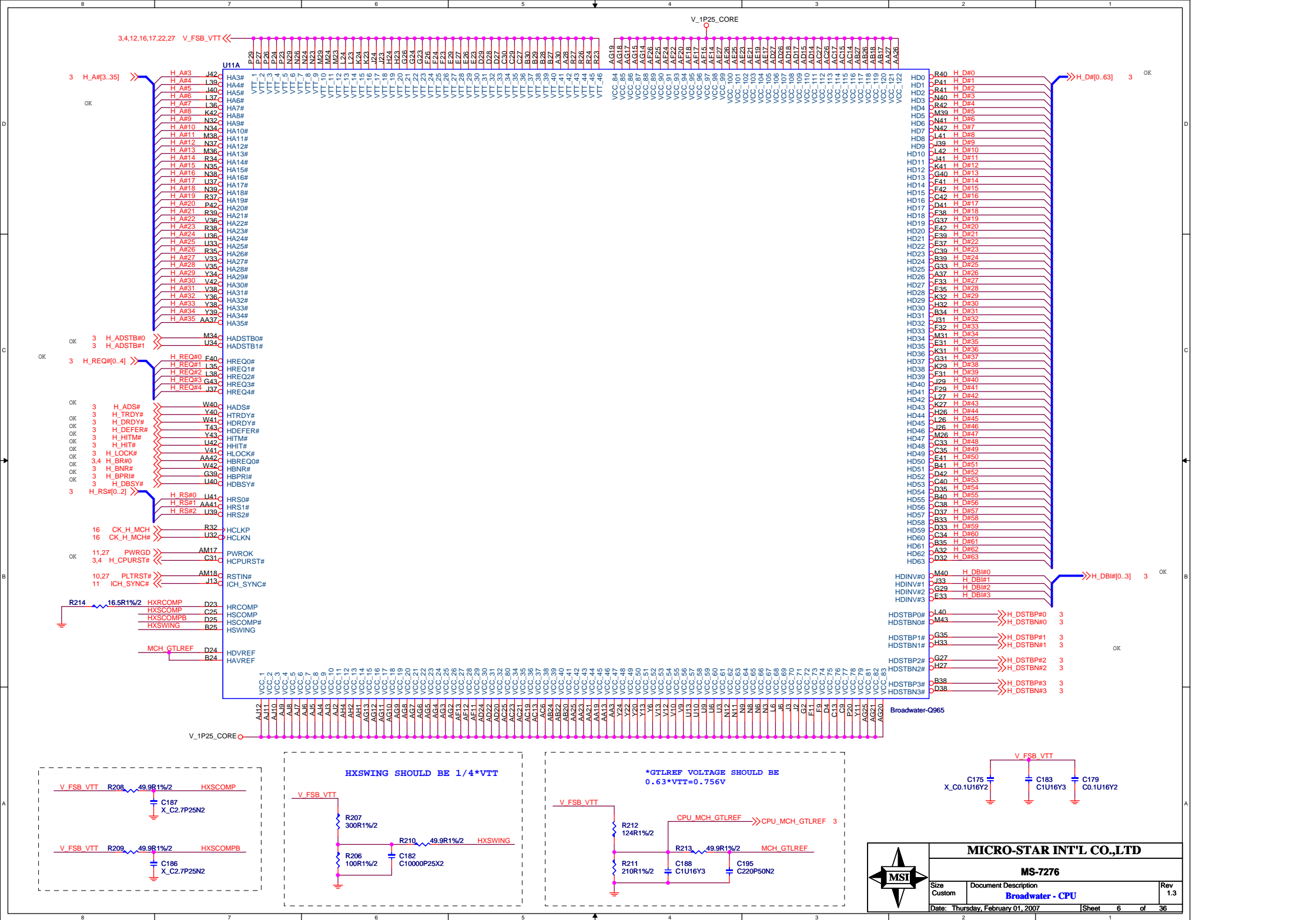


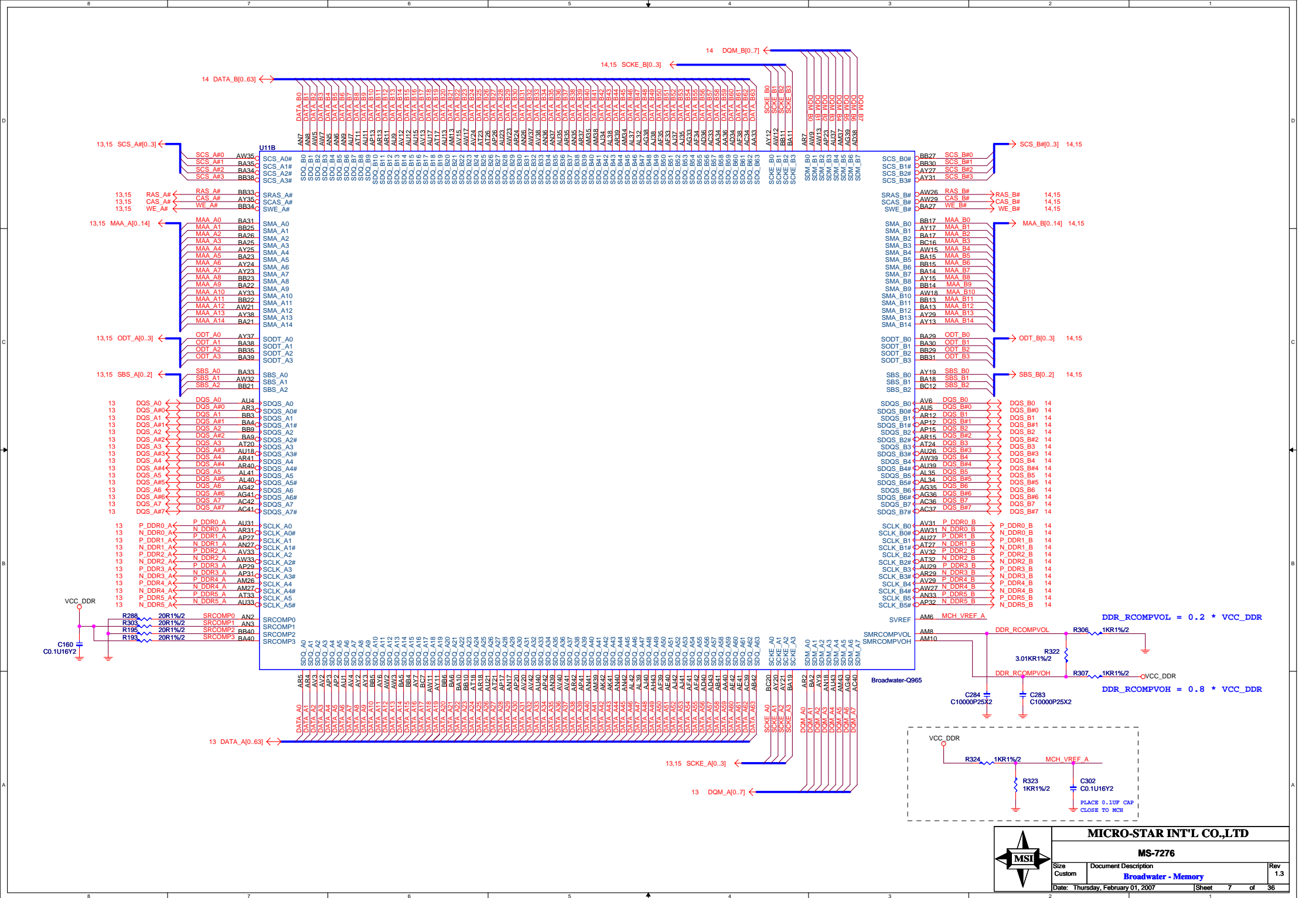
CPU DECOUPLING CAPACITORS



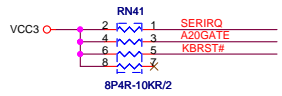
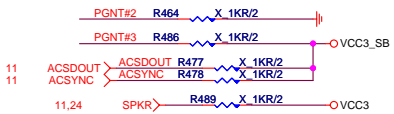
Place these caps within socket cavity

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ICH8 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN/ LAN100_SLP	EN	DIS	INT VRM (VccSus1_05,1_5,VccCL1_5) (VccLAN1_05,VccCL1_05)
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/ PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

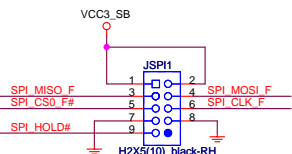


BOOT SELECT STRAPS			
BOOT DEVICE	GNT0	SPI_CS1#	
FWH	1	1	
SPI	0	X	
PCI	1	0	



SPI DEBUG PROT

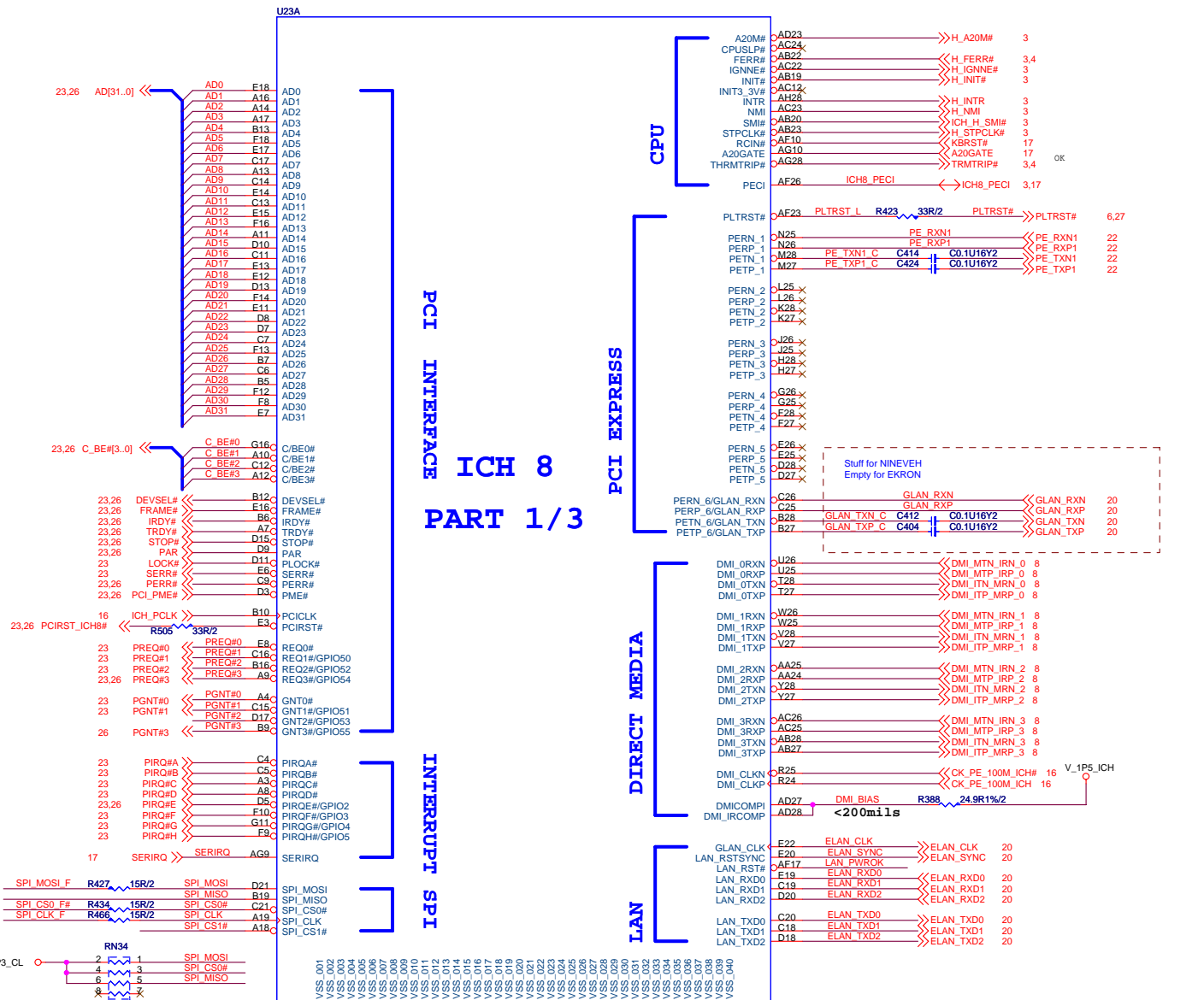
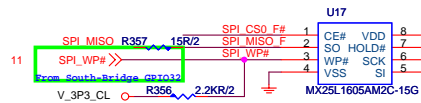
Place close to SPI ROM



Part Number : N31-2051451-H06

SPI FLASH ROM

Place close to SB.



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ICH8 - PCI, DMI, CPU, SPI

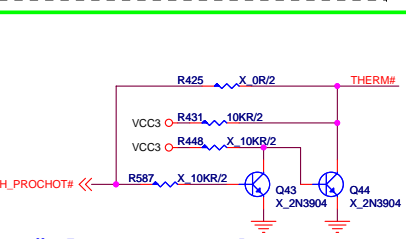
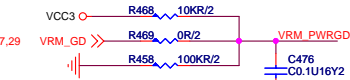
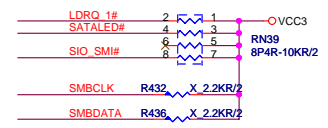
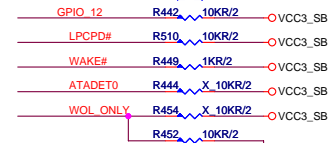
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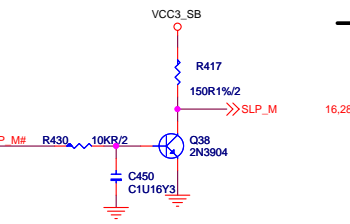
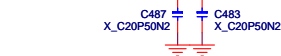
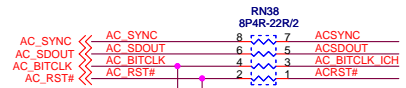
ICH8 PULL-UP RESISTORS

ALL COMPONENTS CLOSE TO ICH8

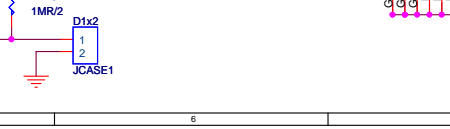
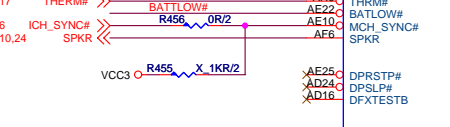
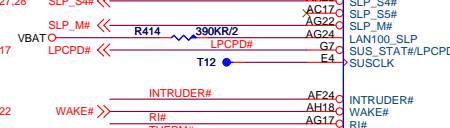
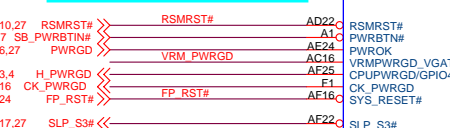
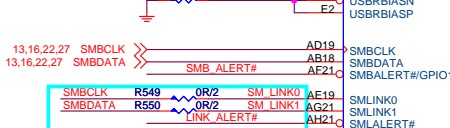
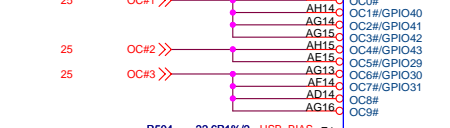
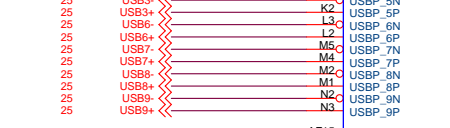
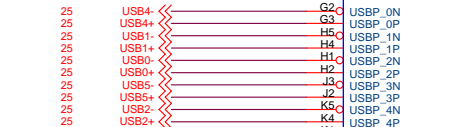
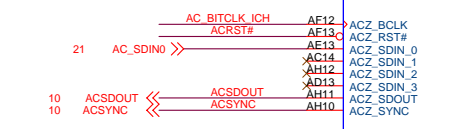
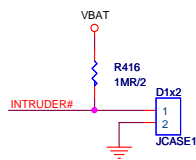
Trace length is less than 3inches to ICH8.



#Place near the SB



Chassis Intrusion



LPC

AC-LINK

USB

SMB

POWER MGMT

MISC

ICH 8 PART 2/3

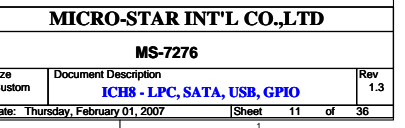
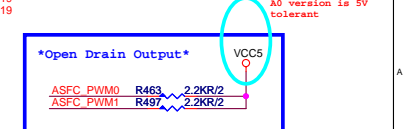
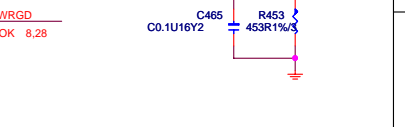
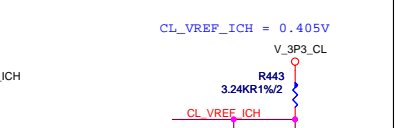
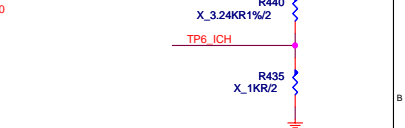
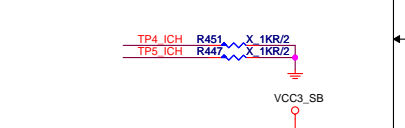
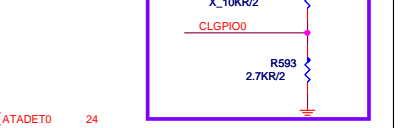
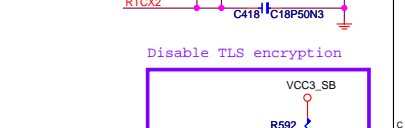
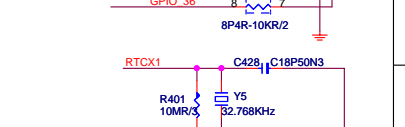
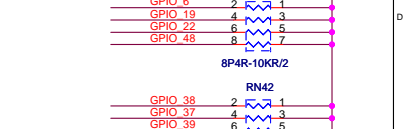
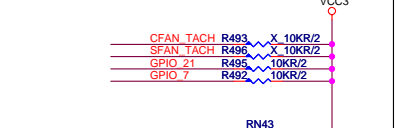
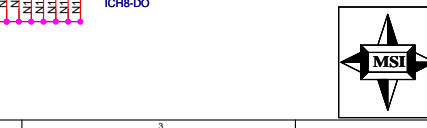
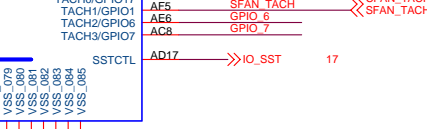
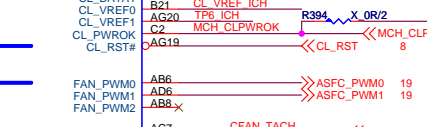
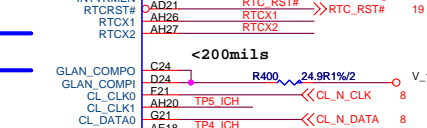
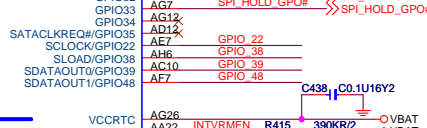
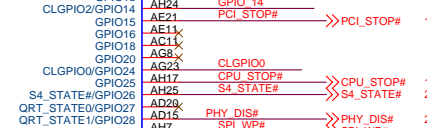
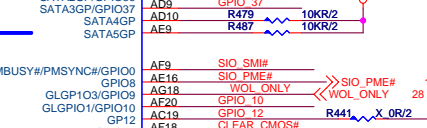
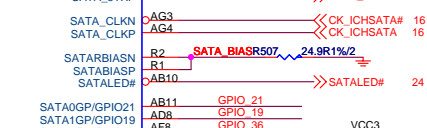
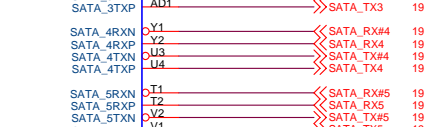
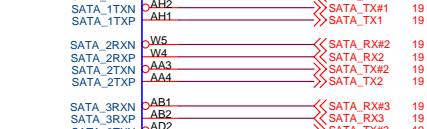
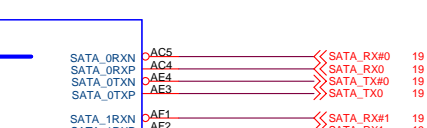
S-ATA

GPIO

RTC

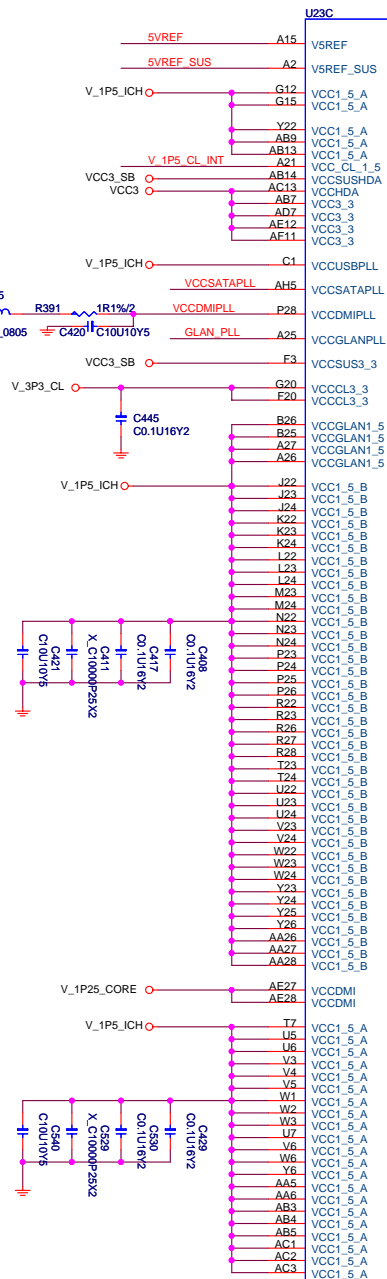
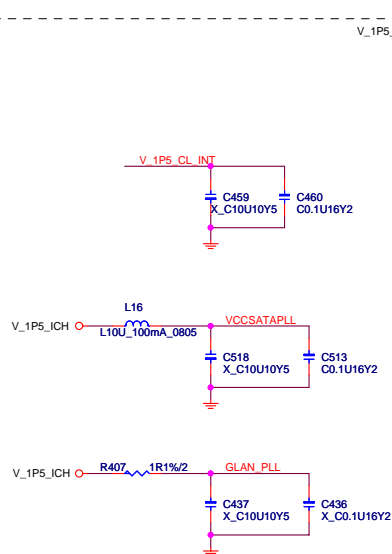
AMT

AFSC



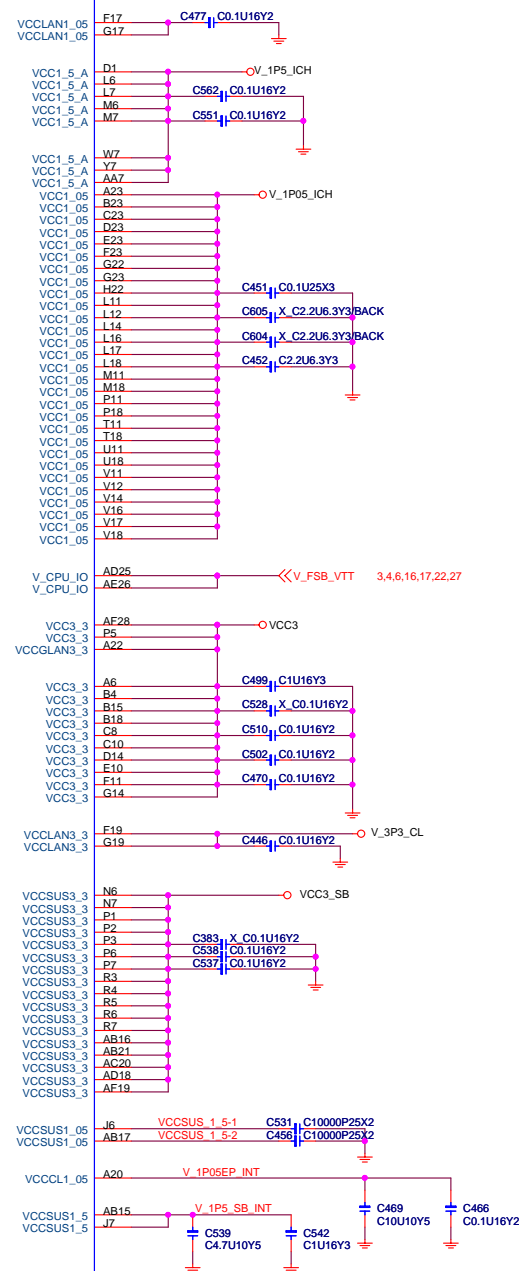
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AD version is 5V tolerant



ICH 8

PART 3/3



ICH8-DO



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Size	Document Description
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ICH8 - POWER

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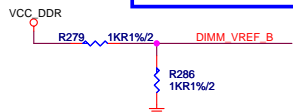
Rev

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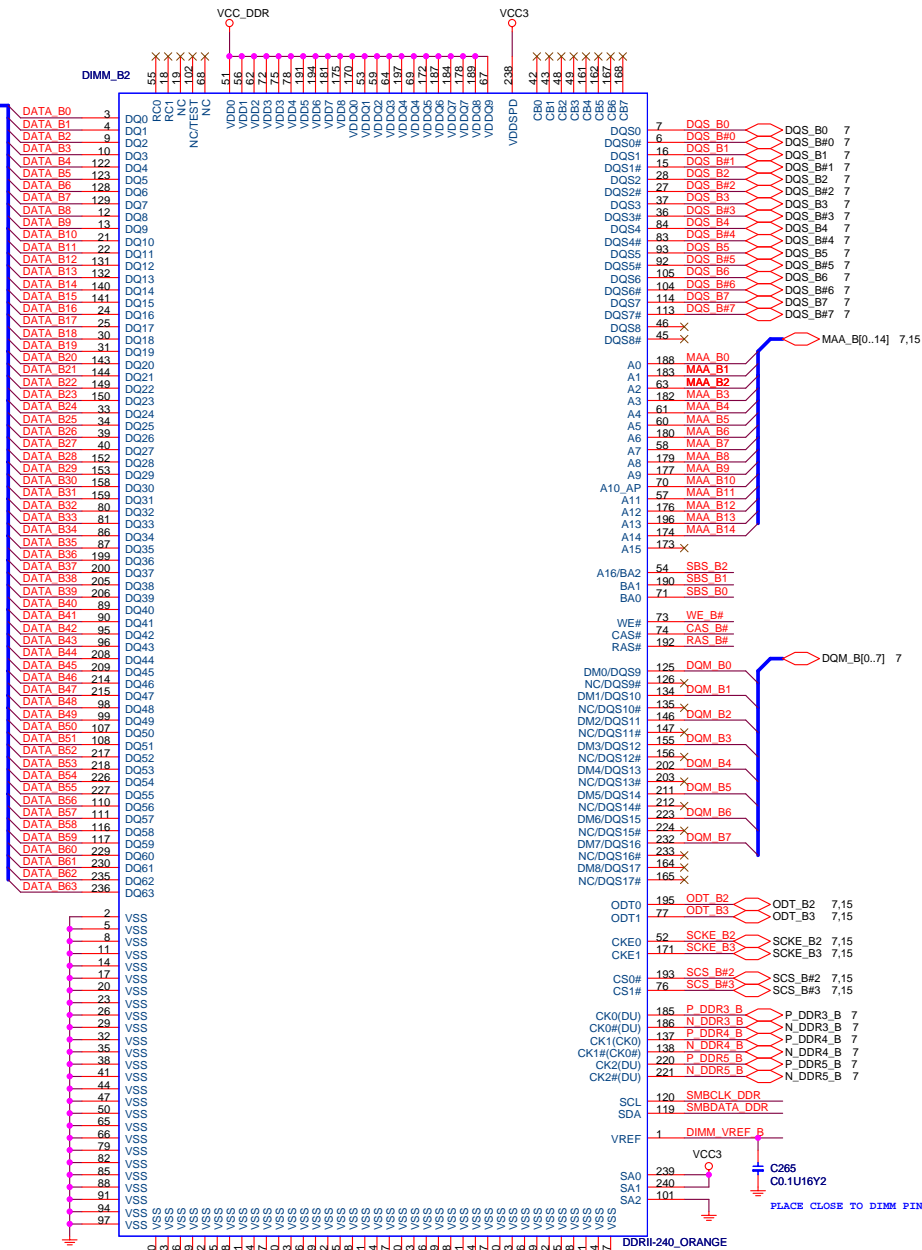


ADDRESS: 010
0xA4

DDRII DIMM_B1



SMBCLK_DDR < SMBCLK_DDR 13
SMBDATA_DDR < SMBDATA_DDR 13



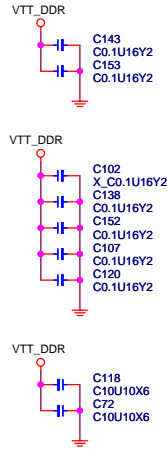
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DDRII DIMM_B2

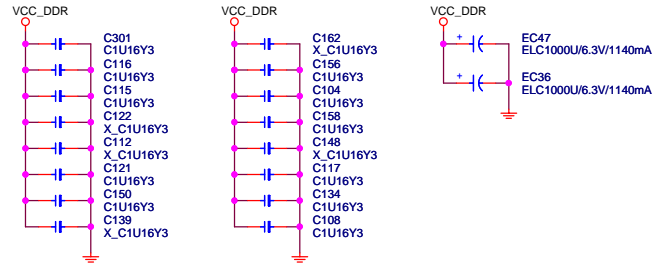
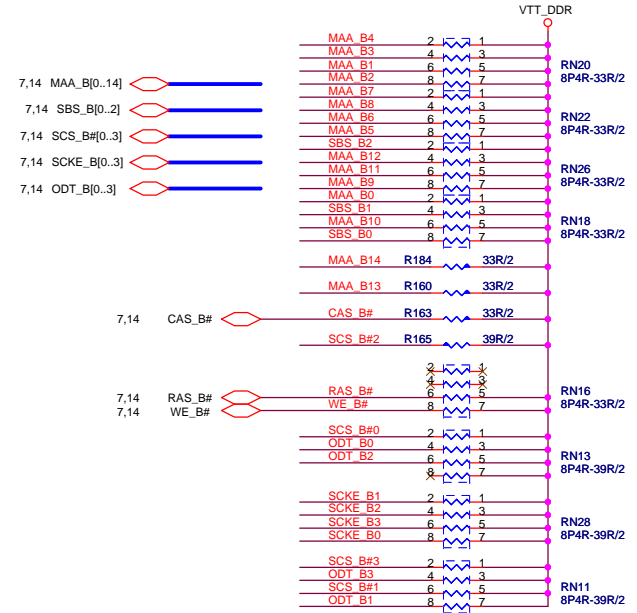
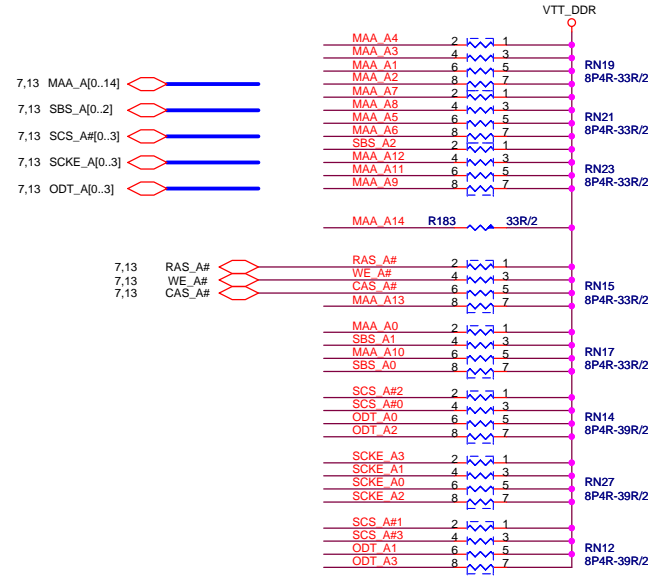
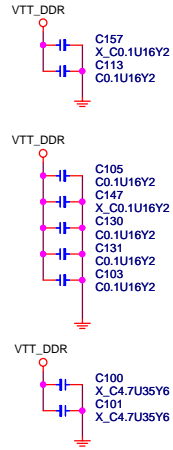


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CHANNEL A V_{SM_VTT}
DECOUPLING CAPS



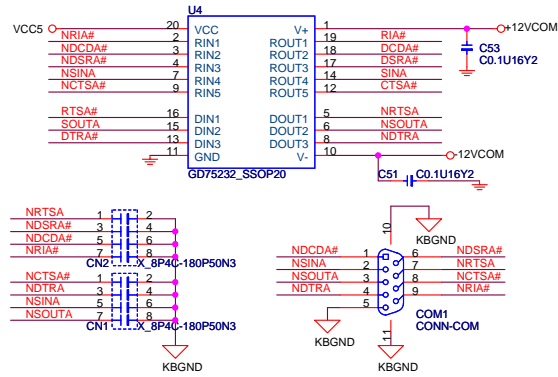
CHANNEL B V_{SM_VTT}
DECOUPLING CAPS



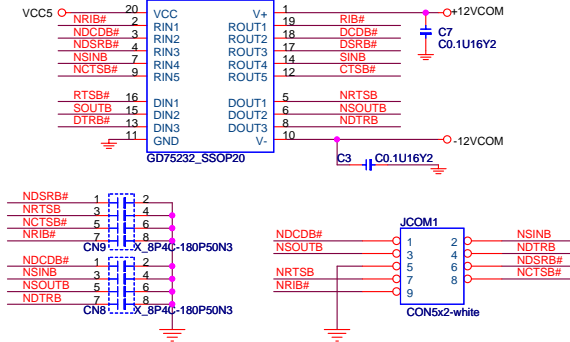
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17 DCDA# >>> DCDA#
17 DSR# >>> DSR#
17 SINA >>> SINA
17 RTSA# >>> RTSA#
17 SOUTA >>> SOUTA
17 CTS# >>> CTS#
17 DTRA# >>> DTRA#
17 RIA# >>> RIA#

17 DCDB# >>> DCDB#
17 DSRB# >>> DSRB#
17 SINB >>> SINB
17 RTSB# >>> RTSB#
17 SOUTB >>> SOUTB
17 CTSB# >>> CTSB#
17 DTRB# >>> DTRB#
17 RIB# >>> RIB#

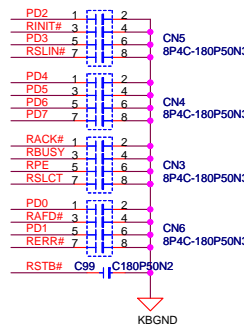
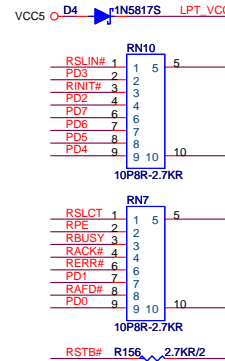


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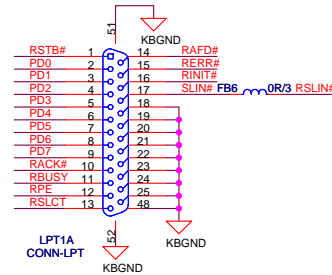


17 PD[7..0] <<< PD[7..0]

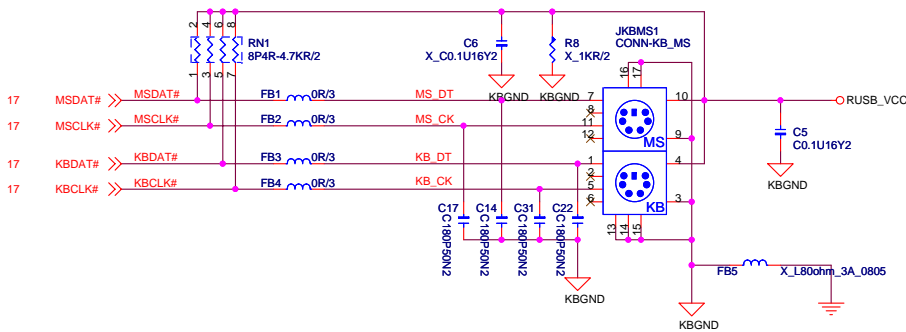
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17 RPE >>> RPE
17 RBUSY >>> RBUSY
17 RACK# >>> RACK#
17 RSLIN# >>> RSLIN#
17 RINIT# >>> RINIT#
17 RERR# >>> RERR#
17 RAFD# >>> RAFD#
17 RSTB# >>> RSTB#



PARALLAL PORT

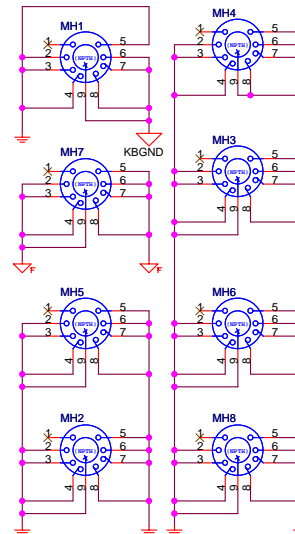


PS2 KEYBOARD & MOUSE CONNECTOR

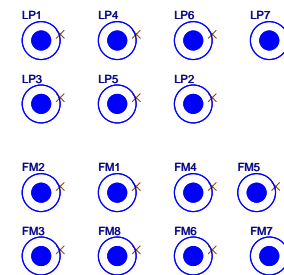


layout時應注意：將KBGND與GND，在第三層用三個50mil的通道相連

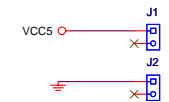
Mounting Holes



Optics Orientation Holes

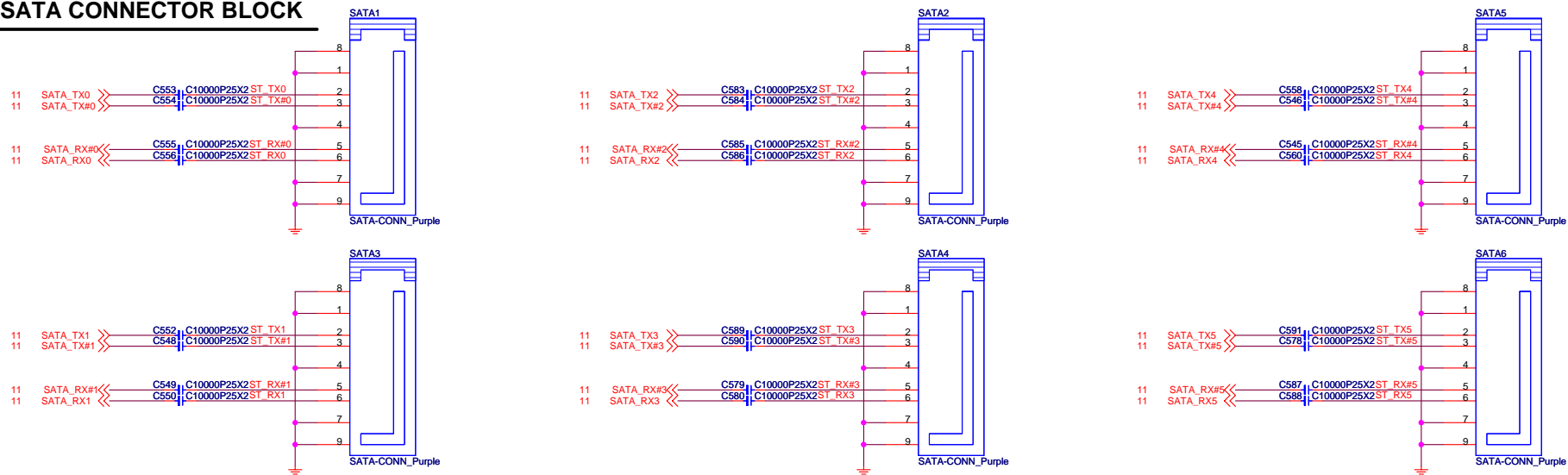


Simulation

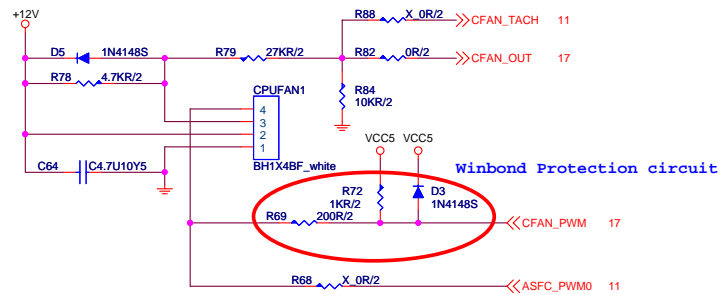


MICRO-STAR INT'L CO., LTD			
MS-7276			
Size	Document Description	Rev	
Custom	PS2 / LPT / COM Port	1.3	
Date: Thursday, February 01, 2007		Sheet	18 of 36

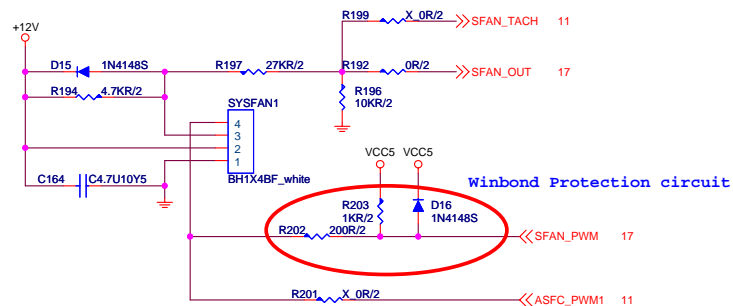
SATA CONNECTOR BLOCK



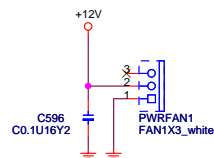
CPU FAN



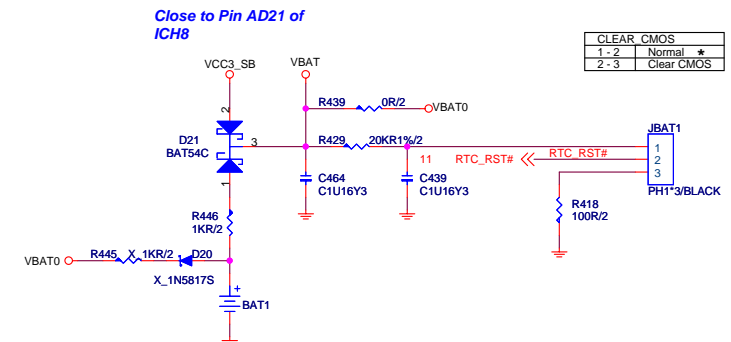
SYSTEM FAN



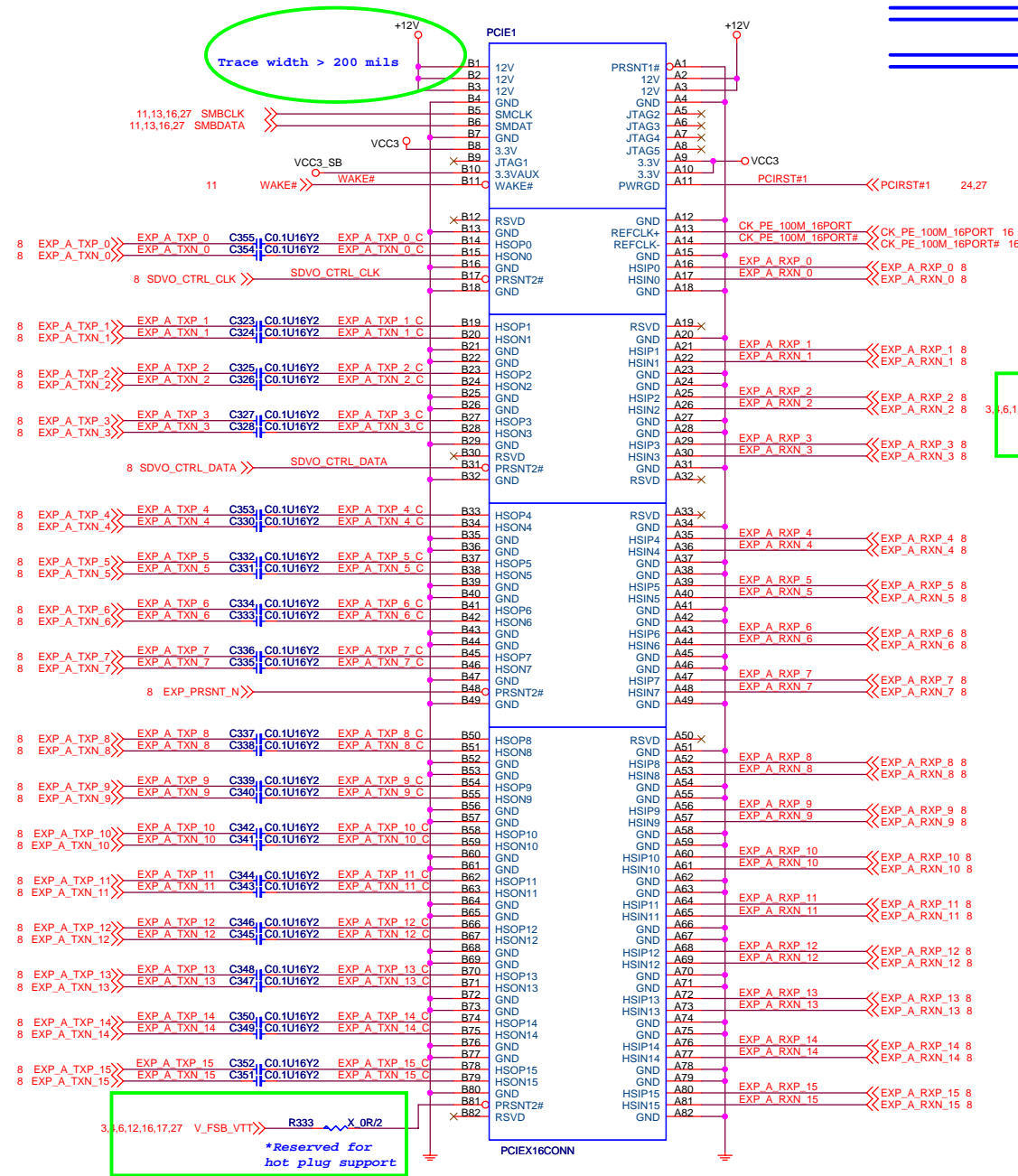
POWER FAN



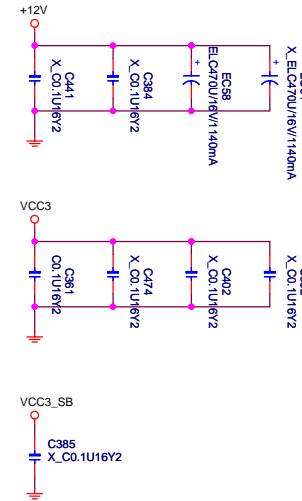
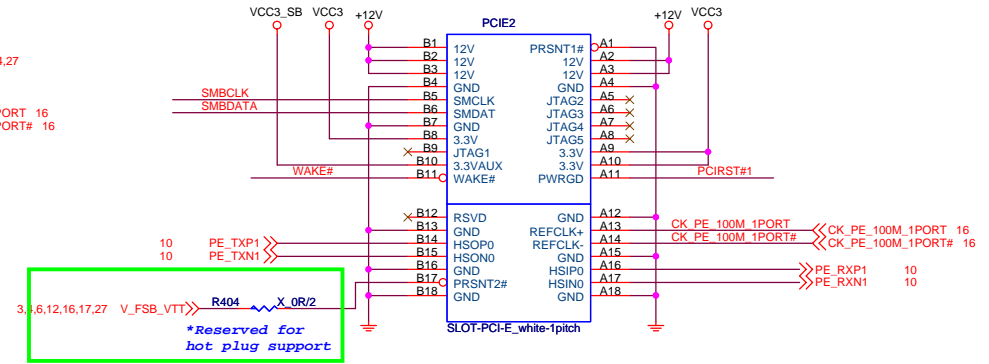
RTC BLOCK



PCI EXPRESS 16-PORT



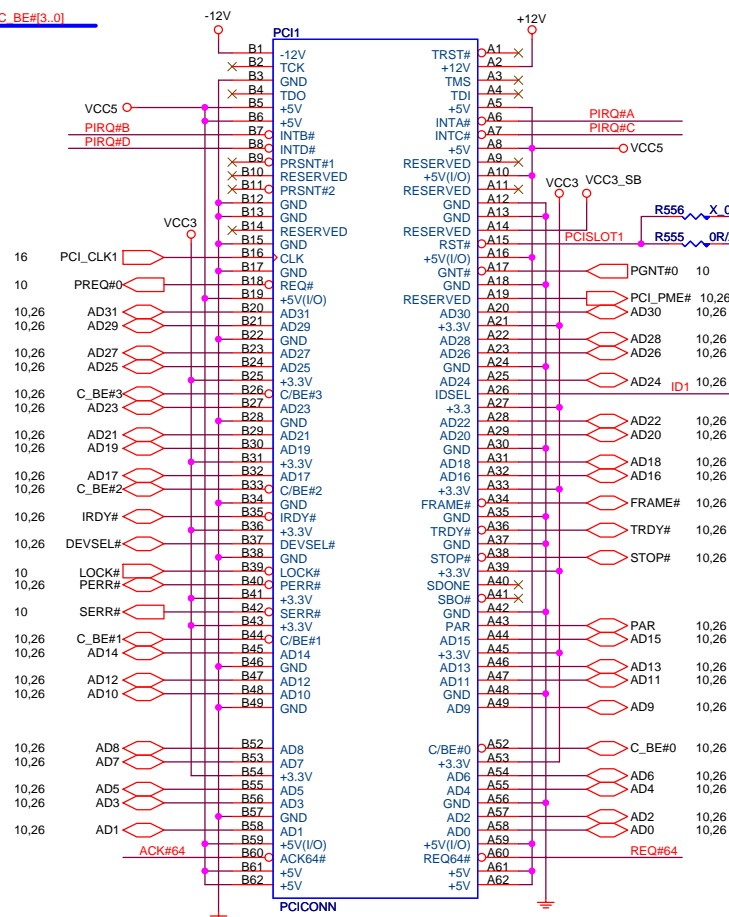
PCI EXPRESS 1-PORT



MICRO-STAR INT'L CO.,LTD		
MS-7276		
Size	Document Description	Rev
Custom	PCIEX16 & PCIE X1 Slot	1.3
Date: Thursday, February 01, 2007	Sheet 22	of 36

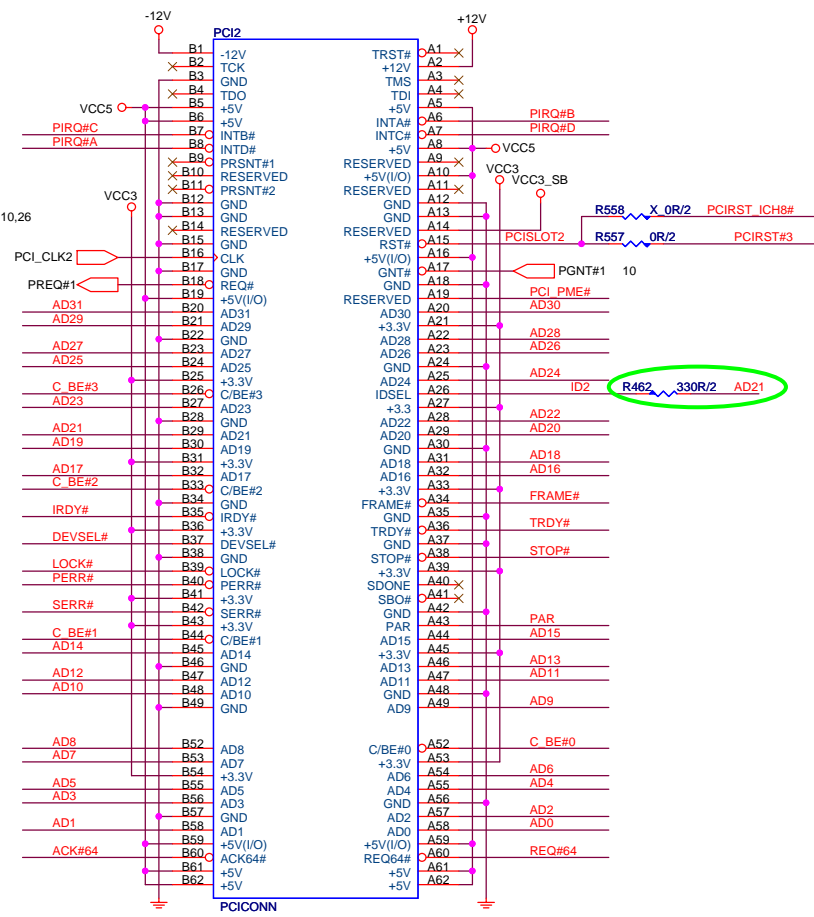
10,26 AD[31..0] << AD[31..0]
10,26 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



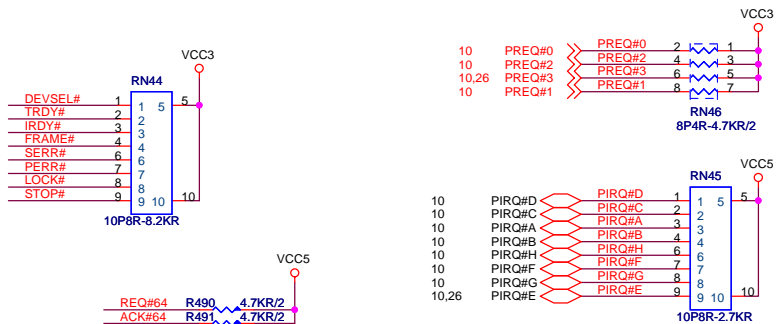
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

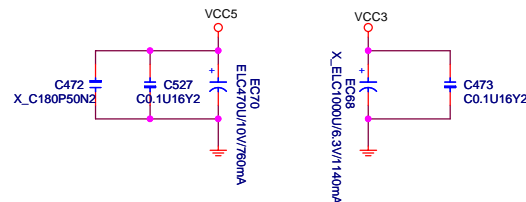


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

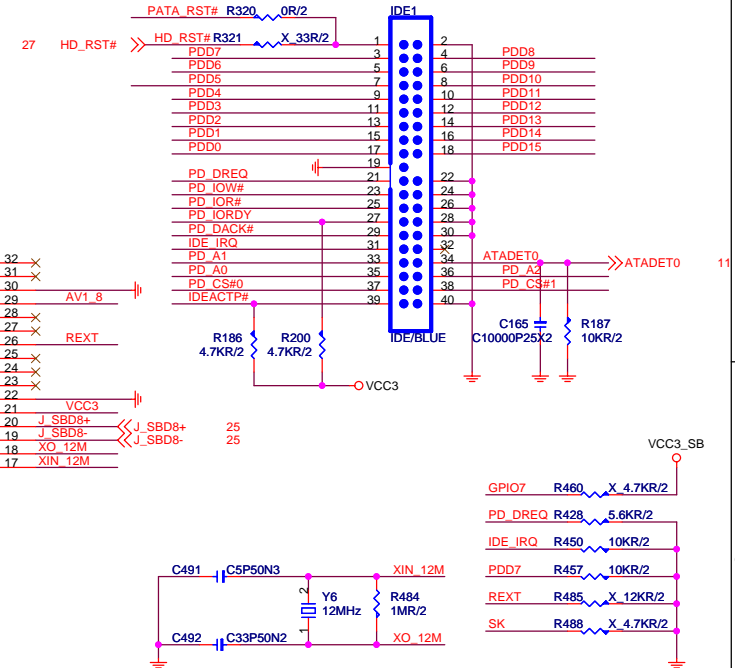
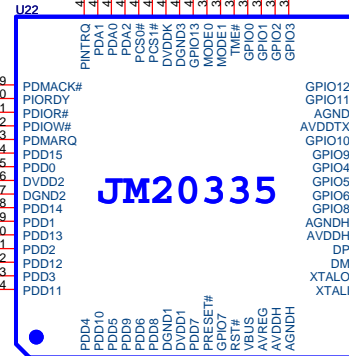
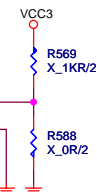
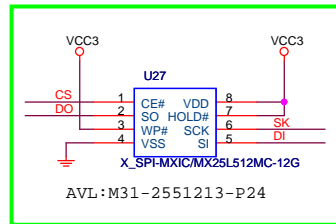
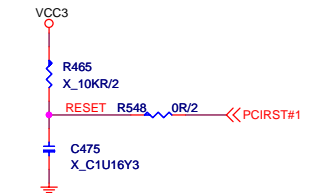
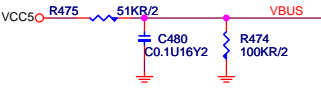
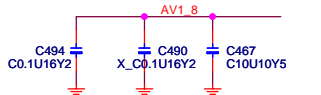
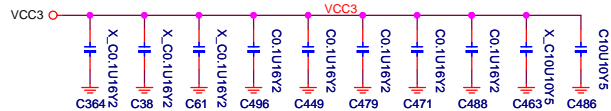


MICRO-STAR INT'L CO.,LTD

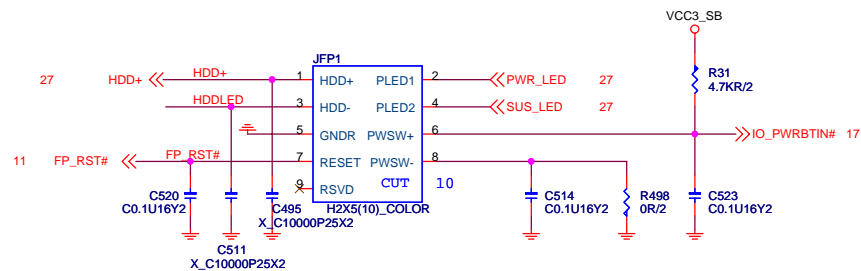
MS-7276

Size	Document Description	Rev
Custom	PCI Slot 1 & 2	1.3
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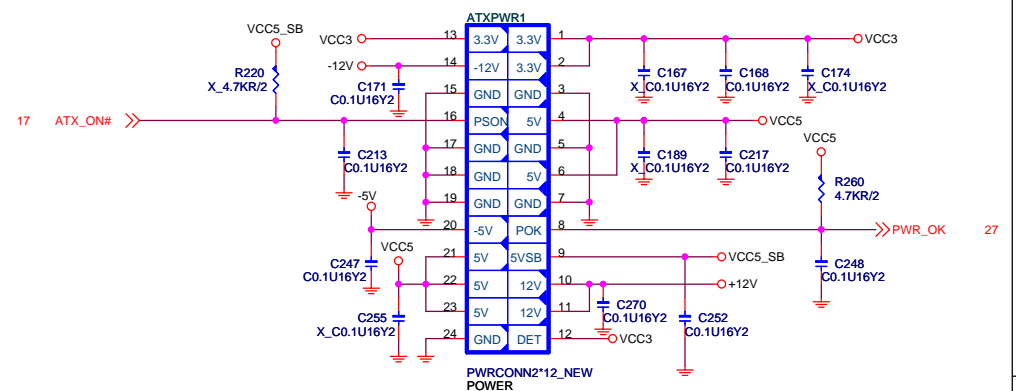
Hi-Speed USB to PATA Bridge



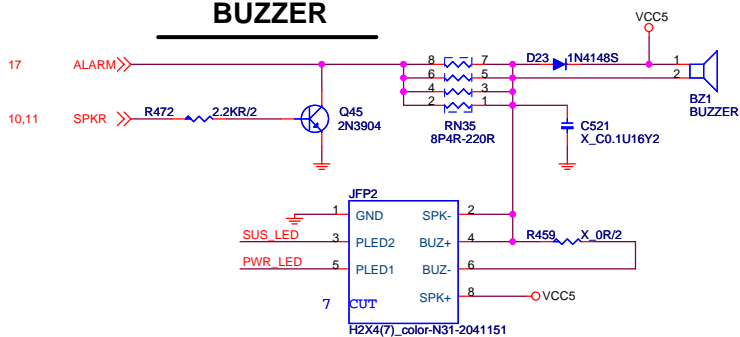
Front Panel



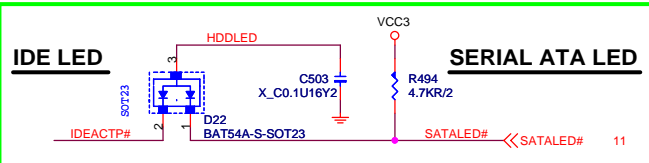
ATX CONNECTOR



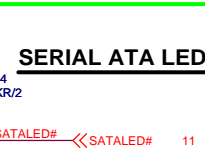
BUZZER



IDE LED



SERIAL ATA LED



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ATX, IDE Connector & F_Panel	1.3
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FS3

2.6A/6V/0.047ohm

R584
X_10K/R2

CS3, CB

OC#1

C0.1U16Y2

Place near SB

R191
27K/R2

R190
51K/R1

R198
1K/R2

RUSB_VCC

NEAR REAR USB CONNECTOR

The schematic diagram illustrates the USB connector circuit. It shows the connection between FUSB_STR, FUSB_VCC1, VCC3_SB, and the NEAR REAR USB CONNECTOR. Components include resistors FS4, R585, R527, R526, R530, and capacitors C483, C592. A note indicates to place C483 near the SB.

[illegible][illegible]

The schematic diagram illustrates the power supply section of the ELC-000000-001/001000. It shows the connection of a 24V AC source through a common mode choke (L20) and a bridge rectifier (BR4R-0R) to a DC-DC converter (U1USD2). The DC-DC converter is powered by a 5V USB source (FUSB_VCC1) and provides a 24V output (V24V) to the rest of the system. The diagram includes pin connections for the choke, rectifier, and converter, as well as the input and output voltages.

Common Mode Choke (L20): The choke has four pins. On the left, pins 8 and 7 are connected to USB5+ and USB6+ (11V), and pins 6 and 5 are connected to USB4+ and USB4- (11V). On the right, pins 4 and 3 are connected to SBD5- and SBD5+, and pins 2 and 1 are connected to SBD4- and SBD4+.

Bridge Rectifier (BR4R-0R): The rectifier has four pins. On the left, pins 1 and 3 are connected to USB4+ and USB5+ (11V), and pins 2 and 4 are connected to USB4- and USB5- (11V). On the right, pins 2 and 1 are connected to SBD4- and SBD4+, and pins 4 and 3 are connected to SBD5- and SBD5+.

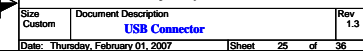
DC-DC Converter (U1USD2): The converter has ten pins. Pin 1 (VCC) is connected to FUSB_VCC1 (5V). Pin 2 (VCC) is connected to SBD5- (11V). Pin 3 (USBD-) is connected to SBD4- (11V). Pin 4 (USBD+) is connected to SBD4+ (11V). Pin 5 (KEY) is connected to GND. Pin 6 (GND) is connected to GND. Pin 7 (USBD-) is connected to SBD5- (11V). Pin 8 (USBD+) is connected to SBD5+ (11V). Pin 9 (GND) is connected to GND. Pin 10 (USBD-) is connected to SBD5- (11V). The output of the converter is V24V (24V).

Input and Output Voltages: The input voltage is 24V AC. The output voltage is 24V DC (V24V).

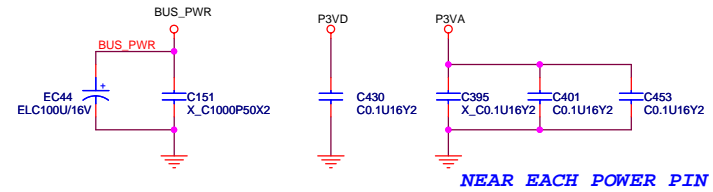
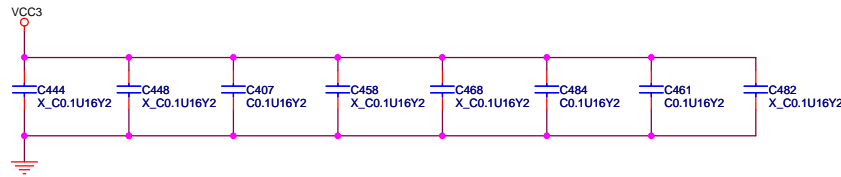
The image contains three circuit diagrams for different USB connectors:

- NEAR USB CONNECTOR:** Shows a USB Type-A connector (D26, IPC2206C/S06) connected to a USB Type-B connector. The USB Type-A pins are labeled 1, 2, 3, 4, 5, 6, 7, 8. The USB Type-B pins are labeled 1, 2, 3, 4, 5, 6, 7, 8. The connector is labeled "X_IPC2206C/S06".
- FRONT USB CONNECTOR FOR USB PORT 8,9:** Shows a USB Type-A connector (R48, B44R-0R) connected to a USB Type-B connector. The USB Type-A pins are labeled 1, 2, 3, 4, 5, 6, 7, 8. The USB Type-B pins are labeled 1, 2, 3, 4, 5, 6, 7, 8. The connector is labeled "X_B44R-0R".
- USB1 connector:** Shows a USB Type-A connector (X_2509/USB Yellow) connected to a USB Type-B connector. The USB Type-A pins are labeled 1, 2, 3, 4, 5, 6, 7, 8. The USB Type-B pins are labeled 1, 2, 3, 4, 5, 6, 7, 8. The connector is labeled "X_2509/USB Yellow".

Diagram illustrating the connection of RS08 and RS09 to the P-ATA bus. RS08 is connected to OR/2 and RS09 to OR/2. The output of RS08 is J_SBD+ and the output of RS09 is J_SBD-. The bus is labeled P-ATA.

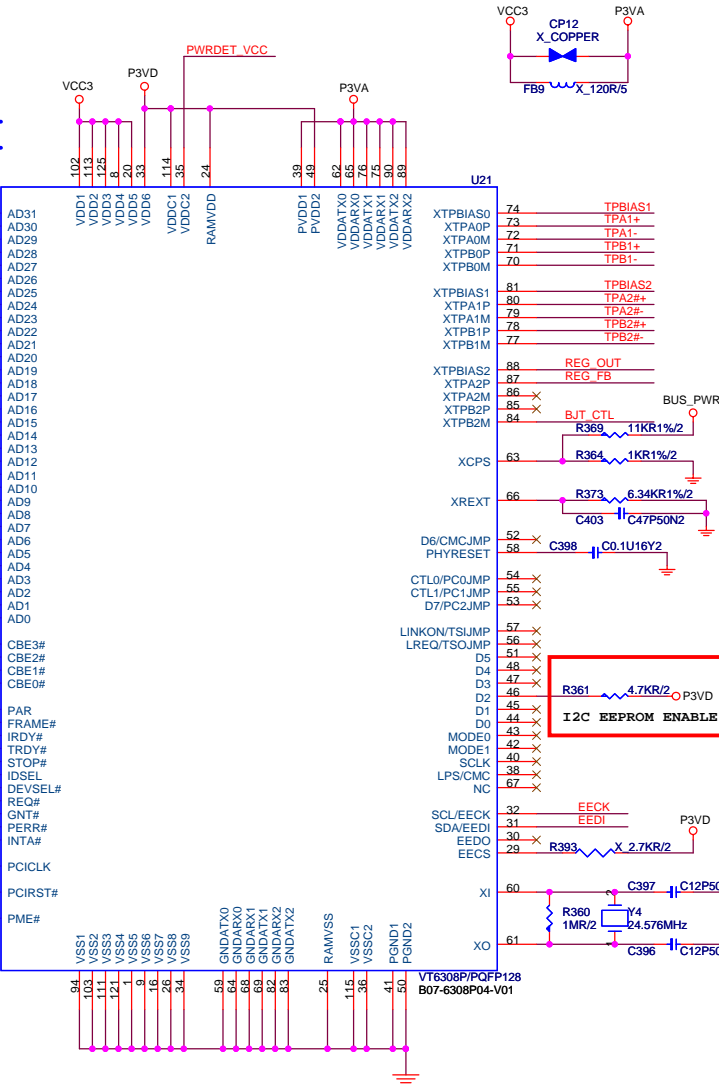


IEEE-1394

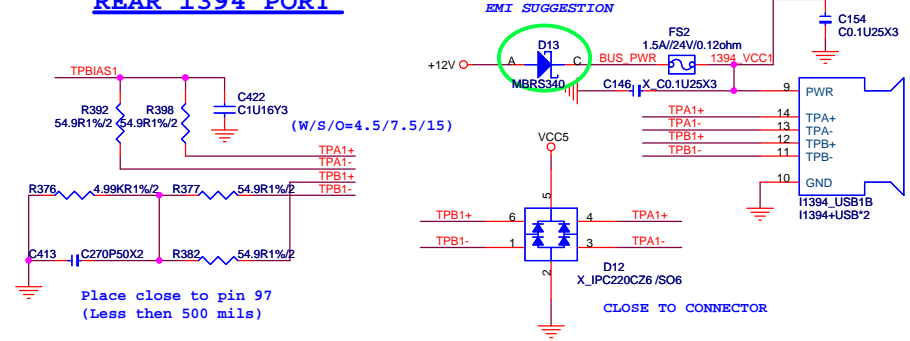


NEAR EACH POWER PIN

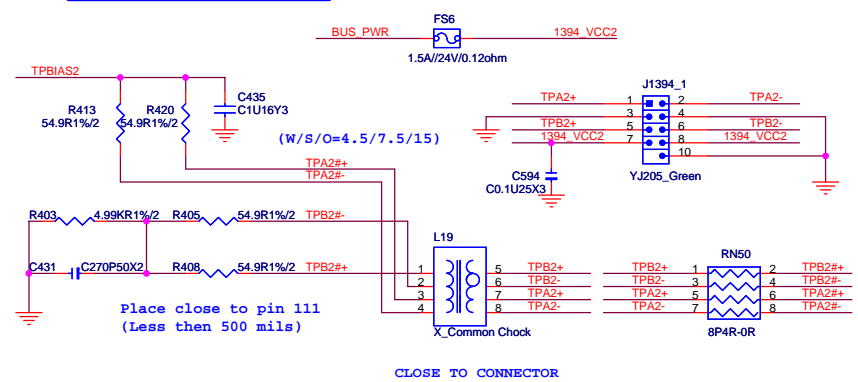
10,23 AD[31:0] AD[31:0]
10,23 C_BE#[3:0] C_BE#[3:0]



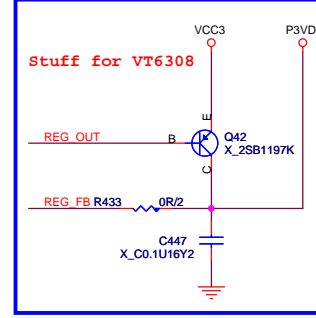
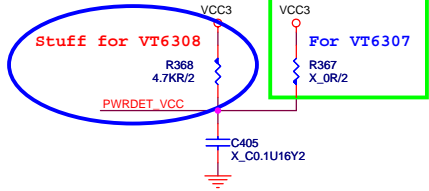
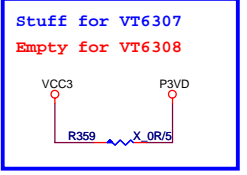
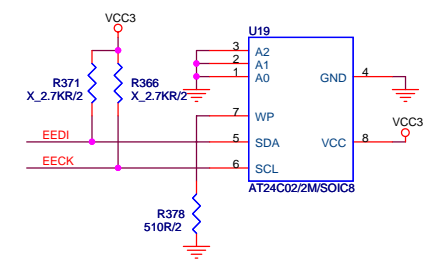
REAR 1394 PORT



FRONT 1394 PORT



1394-EEPROM 24C02



ACPI Controller MS-7

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

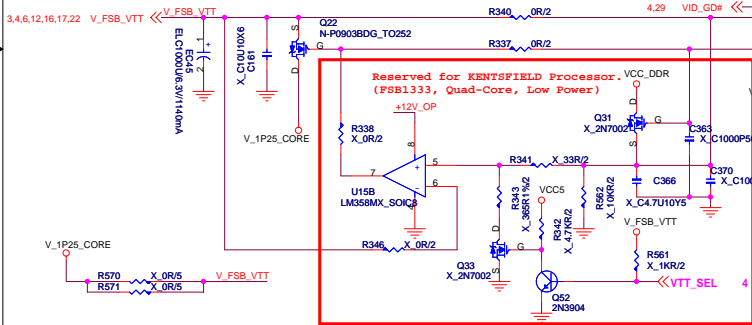
3VSB MODE SELECT

3VSB MODE	3VdLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

DDR I & DDR II VOLT SELECT

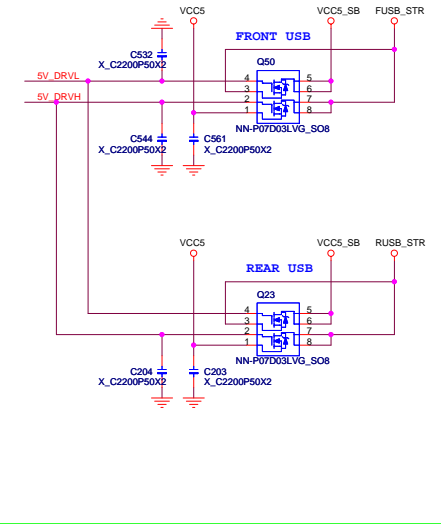
DDRTYPE	VdIMM
PULL LOW	2.5V
PULL HIGH	1.8V

V_FSB_VTT 6.2A

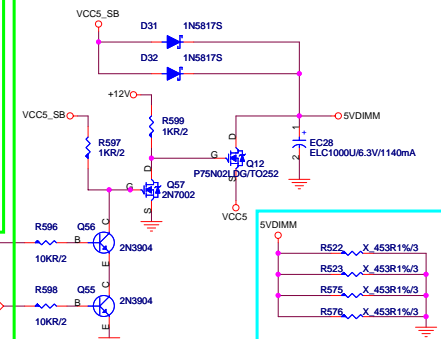


VTT_SEL = H	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = L	V_FSB_VTT=1.2V	For normal processors.

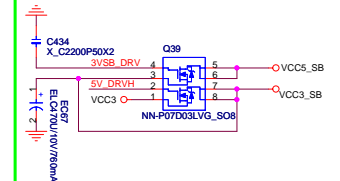
5V DUAL Power 5A



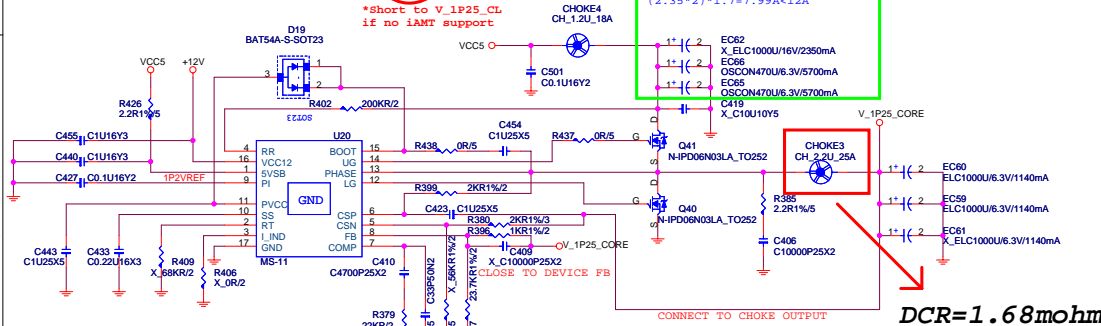
5VDIMM



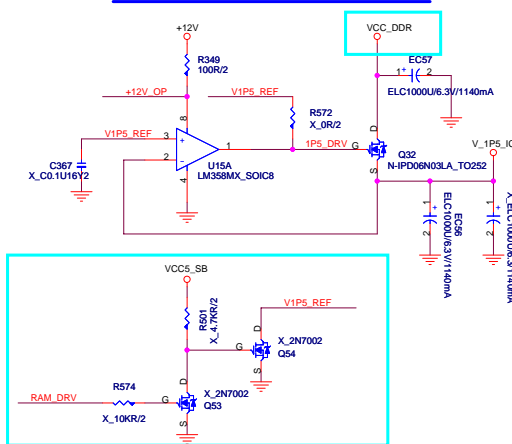
VCC3_SB Power



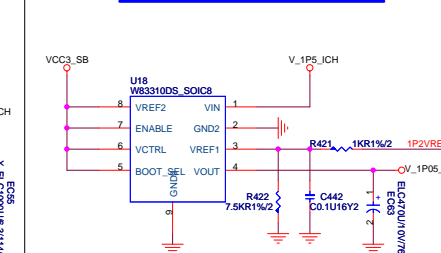
V_1P25_CORE POWER...21.34A + 3.8A



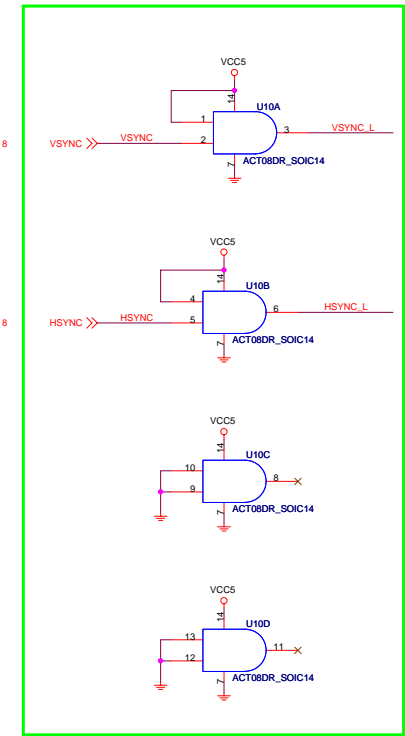
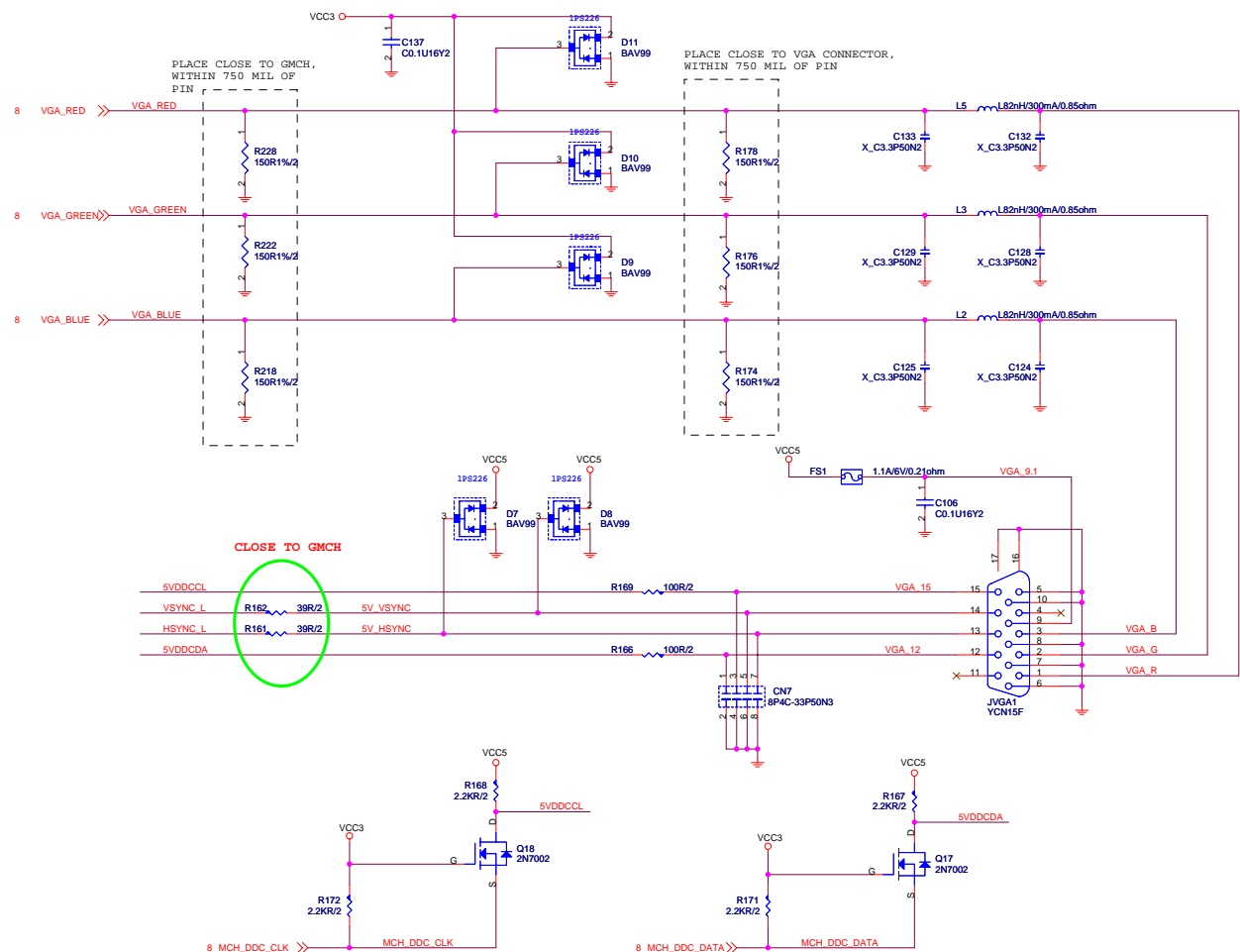
V_1P5_ICH...2A + 1.17A



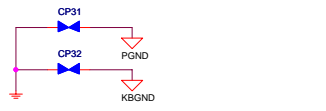
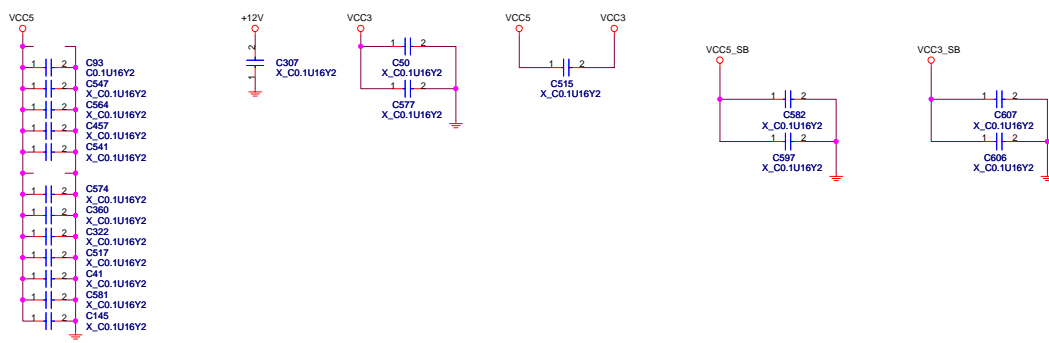
V_1P05_ICH...1.17A



Video Connector



EMI Reserved



ICH8

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO_SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN_TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO_[7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO_PME#
GPIO[9]	WOL_EN		I/O	Resume	Y	Y	3.3V	Native	GPIO_9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO_10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB_ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR_CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO_14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN_TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO_19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO_21
GPIO[22]	SCLOCK		I/O	Core	Y		3.3V	GPI	GPIO_22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT_IO#
GPIO[26]	S4_STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL_STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL_STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO_36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO_37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO_38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO_39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO_48
GPIO[49]	CPUPWRGD		I/O	V_CPU_IO			CPU	Native	H_PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD21	PCI_CLK2
1394	PIRQ#D	PREQ#3 PGNT#3	AD22	1394_PCLK

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI_E X16 & PCI_E X1
PCIRST#2	SIO, 1394, FWH, TPM
PCIRST#3	PCI SLOT1&2,
PCIRST_ICH8#	MS7
HD_RST#	Primary IDE

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
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0A modify 10 change list

1. Add R536 for SLP_M
2. Q30.C connect to U8.10
3. change VTT_DDR driven from VCC_DDR
4. modify ALC883 circuit to meet the Vista "premium" SPEC
5. 1394 circuit modify, change net name from "VDD" to "P3VD" (page 26)
4. modify ALC883 circuit to meet the Vista "premium" SPEC
5. modify JM20335 circuit (page 24)
6. modify SMBLINK and SMBCLK/DATA circuit (page 11)
7. add C469 C539 for margin (page 12)
8. add R564 and R563 for ICS (page 16)
9. CPU FAN mornitor from AUXFANOUT change to CPUFANOUT1 (page 17)
10. add R566 and R567 for JM20335 (page 25)
11. modify V_FSB_VTT circuit (page 27)
12. change R51 R3 R62 R10 to 0ohm for power team solution (page 29)
13. modify V_1P5_ICH circuit from Vcc3 change to VCC_DDR (page 27)
14. Add Q54 and Q53 for S3 sequence (page 27)
15. reserve R522 R523 R575 R576 預防逆向電流 (page 27)
16. add R578 R579 R580 R581 R582 R583 for 48M and 14M pull high and pull down (page 16)
17. Add C606 C607 for EMI (page 30)
18. Add R584 R585 R586 for option USB OC# function (page 25)
19. change C369 and C371 footprint to 0805 (page 20)
20. change 1394`s PCIREST to PCIREST_ICH8 (page 26)

10 modify 11 change list

1. change 1394`s IRQ to PIRQ#E (page 26)
2. modify JM20335 circiut (page 24)
3. Add C498 and C500 for EMI (pang 29)
4. change R578 R579 R582 pull high to VCC3V (page 16)
5. Add C507 between USB8+ and USB8- (pang 25)
6. Add C508 between GNDF and PGND for EMI (pang 21)
7. Add R591 for winbond AP note (pang 17)
8. SWP CPUCLK and MCHCLK (pang 16)
9. change I2C pull up rail to VCC3_SB,stuff R551 R552, non-stuff R432 and R436 (pang 11)

1.1 modify 1.11 change list


1. Add R592、R593 for disable TLS encryption (page 11)
2. Add R594、R595 for select SLP_S4# or S4_STSTE# (page 27)
3. Add R350、R600 for RAM_VREF, please close to MS11(U8) (pang 28)
4. Modify MS7 circuit for 5VDIMM (page 27)

11/07 modify BOM for meet VRD11 based on 7276-21

1. Change R26 from 2.4k to 1.91k ohm . (Page 29)
2. Change R30 from 20k to 15k ohm. (Page 29)
3. Stuff 100 ohm in R29. (Page 29)
4. Stuff 470p in C29. (Page 29)
5. Non-stuff R40. (Page 29)
6. Stuff 41.2K ohm in R38. (Page 29)
7. Change R58 from 120k to 100k ohm. (Page 29)
8. Stuff 560uF in EC38. (Page 29)

1.11 modify 1.3 change list

1. Change Chassis Intrusion circuit with ICH8 . (Page 10)



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